ABSOLUTE BINARY PROGRAM NO. 12936-16001

PRIVILEGED INTERRUPT FENCE DIAGNOSTIC

for

hp-2100A/S AND 21MX COMPUTERS

reference manual

NOTICE

The absolute binary code for this diagnostic is contained on one or more media (e.g., paper tape, cartridge tape, disc, and magnetic tape). The binaries also exist on single as well as multiple files. For the current date code(s) associated with these media, refer to appendix A in the *Diagnostic Configurator Manual,* part no. 02100-90157, dated August 1976 or later.

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SECTION I
INTRODUCTION

1-1. GENERAL

The HP 12936 Privileged Interrupt Fence Diagnostic confirms proper operation of the HP 12936 Privileged Interrupt Fence PCA (Printed-Circuit Assembly). This diagnostic is one of the 2100 series computer system diagnostics executed in conjunction with the HP 2100 Series Diagnostic Configurator. Test sequence and test failure reporting to the operator is provided through a console (if available), through the computer Memory Data Register (sometimes referred to as the T-register), and the A-register.

Operator input is required via the switch register for test options and via the A-register for individual test selection. The PRESET switch(es) are pressed by the operator to test the preset function.

The diagnostic consists of nine tests which test all four functional states of the Privileged Interrupt Fence and one troubleshooting scope loop test.

1-2. REQUIRED HARDWARE

The following hardware is required:

a. This diagnostic may be executed in any of the following computers with at least 4K of memory:

   (1) 2100A/S.

   (2) 21MX M-Series:* 2105, 2108, or 2112 computer.

   (3) 21MX E-Series:* 2109 or 2113 computer.

b. A console device is optional for error and message reporting.

c. A diagnostic input device as specified in the *Diagnostic Configurator Reference Manual* is to be used to load the Configurator and the diagnostic program.

d. Two standard I/O** interfaces with flag, control, and interrupt circuitry (including the console device interface) must be used to test I/O related functions above and below the SC

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*21MX M-Series and 21MX E-Series will be referred to as 21MX throughout this reference manual.

**Standard I/O implies that the interface will respond to the assigned meaning of the I/O instructions and will also interrupt when the Control and Flag are set and the interrupt system is enabled.

of the Privileged Interrupt Fence. The terms "low SC" and "high SC" are employed throughout this manual to specify the two I/O interface PCA's. The term "low SC" is synonymous with high priority channel and the term "high SC" is synonymous with low priority channel. If a console interface PCA is used, the first characters may be scrambled when information or error messages are outputted to the console. If a teleprinter interface PCA is used, do not attempt to use Scope Loop Test 09. Test 09 causes the teleprinter to chatter because Control and Flag flip-flops are constantly being set and cleared.

e. The HP 12936 Privileged Interrupt Fence PCA is required.

f. I/O jumpers must be installed to effect unbroken priority.

1-3. REQUIRED SOFTWARE

The following software is required:

a. Diagnostic Configurator used for equipment configuration and as a console driver:

   Absolute Binary Program, part no. 24296-60001
   Reference Manual, part no. 02100-90157

b. Privileged Interrupt Fence Diagnostic (HP 12936-16001).

Since the two I/O interface PCA's must be in working order, it is recommended that diagnostics, which correspond to each PCA, be executed prior to running the Privileged Interrupt Fence Diagnostic.

The diagnostic serial number of the Privileged Interrupt Fence Diagnostic which resides in memory location 126 is 103115.

PROGRAM ORGANIZATION

SECTION II

2-1. ORGANIZATION

This diagnostic consists of an Initialization section, a Control section, nine standard tests, and a scope loop test. The Initialization section prepares the diagnostic with the test select code and options specified by the operator.

2-2. TEST CONTROL AND EXECUTION

The Control section is responsible for printing an introductory header message on the console (if available) and then executing tests according to the options selected in the Switch Register. These options are fully defined in the following sections. (Refer to table 3-3.) The Control section also keeps count of the number of completed test passes and, if Switch Register bit 10 is clear, will output the pass count to the console device.

2-3. MESSAGE REPORTING

If a console device is used, two types of messages are reported: error and information.

Error messages are used to inform the operator if the privileged interrupt fence or either of the selected interface PCA's have failed to properly execute a function or if the priority chain is broken.

Information messages are used to instruct the operator to perform an operation related to the diagnostic's function or to inform him of the progress of the diagnostic. An Information halt will occur to allow the operator an opportunity to perform a function. A printed message will be preceded by an E (error) or H (information) and an octal number which relates to a halt code (last two octal digits only). An example of an error message follows:

Error Halt

Message: E052 FENCE INT'D AFTER LO SC INT'D WITH FENCE CONTROL SET
Halt Code: 102052 (octal)

Error messages can be suppressed by setting Switch Register bit 11. Error halts can be suppressed by setting Switch Register bit 14. Information messages may be suppressed by setting Switch Register bit 10.

OPERATING PROCEDURES

SECTION III

3-1. CONFIGURATION

Ensure that the two standard interface PCA's (as listed in paragraph 1-2d) and the Privileged Interrupt Fence PCA are installed as follows: The SC of the first standard interface PCA must be less than the SC of the Privileged Interrupt Fence PCA which must be less than the SC of the second standard interface PCA. The priority chain from SC 10 to the SC of the second standard interface PCA must be maintained. A flowchart of the diagnostic operating procedure is provided in figure 3-1.

3-2. ILLEGAL TRAP CELL HALTS

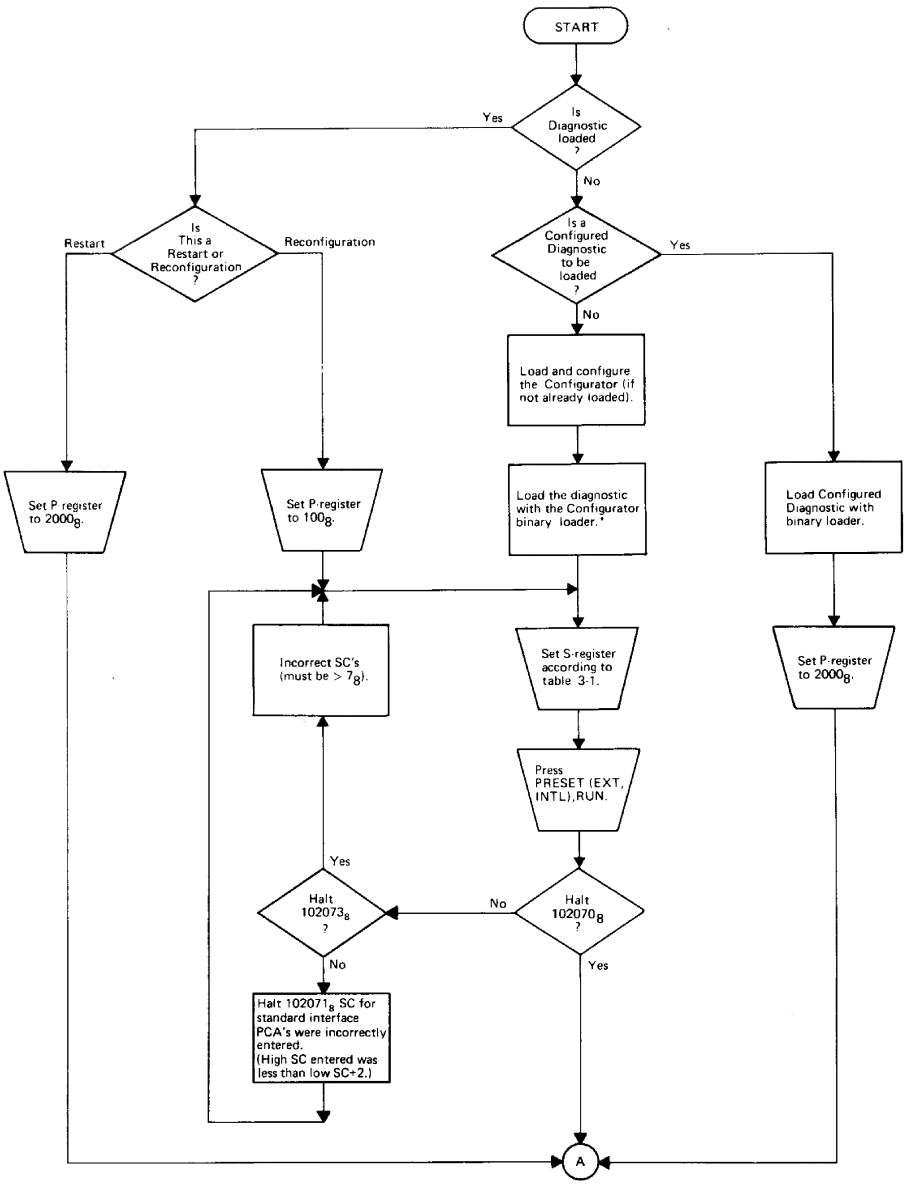
If an illegal trap cell halt (106077) occurs during the diagnostic execution, the operator must determine the source of the failure by inspecting the P-Register and M-Register. (The operator can recover by restarting the program as described in figure 3-1.) The program may have to be reloaded.

3-3. TEST SELECTION BY OPERATOR

The Control section allows the operator the option of selecting a test or sequence of tests to be executed. The operator sets Switch Register bit 9 to indicate that he wants to make a selection and then presses RUN. The computer will come to a halt 102075 (octal) to indicate it is ready for the selection. If the program is running, the test in progress will be completed and then the program will halt. Now the operator loads the A-Register with the test(s) desired. A-Register bit 0 represents test 00, bit 1 represents test 01, and so on up to bit 9 which represents test 09. The operator must now clear Switch Register bit 9 and press RUN. The operator-selected test(s) will then be run.

Table 3-1. Entry of First and Second Interface SC's via Switch Register

S-REG BITS	FUNCTION
15-12	Reserved.
11-6	SC of second standard interface PCA (greater than SC of Privileged Interrupt Fence PCA).
5-0	SC of first standard interface PCA (less than SC of Privileged Interrupt Fence PCA).



12936-1

Figure 3-1. Operating Procedure Flowchart (Sheet 1 of 2)

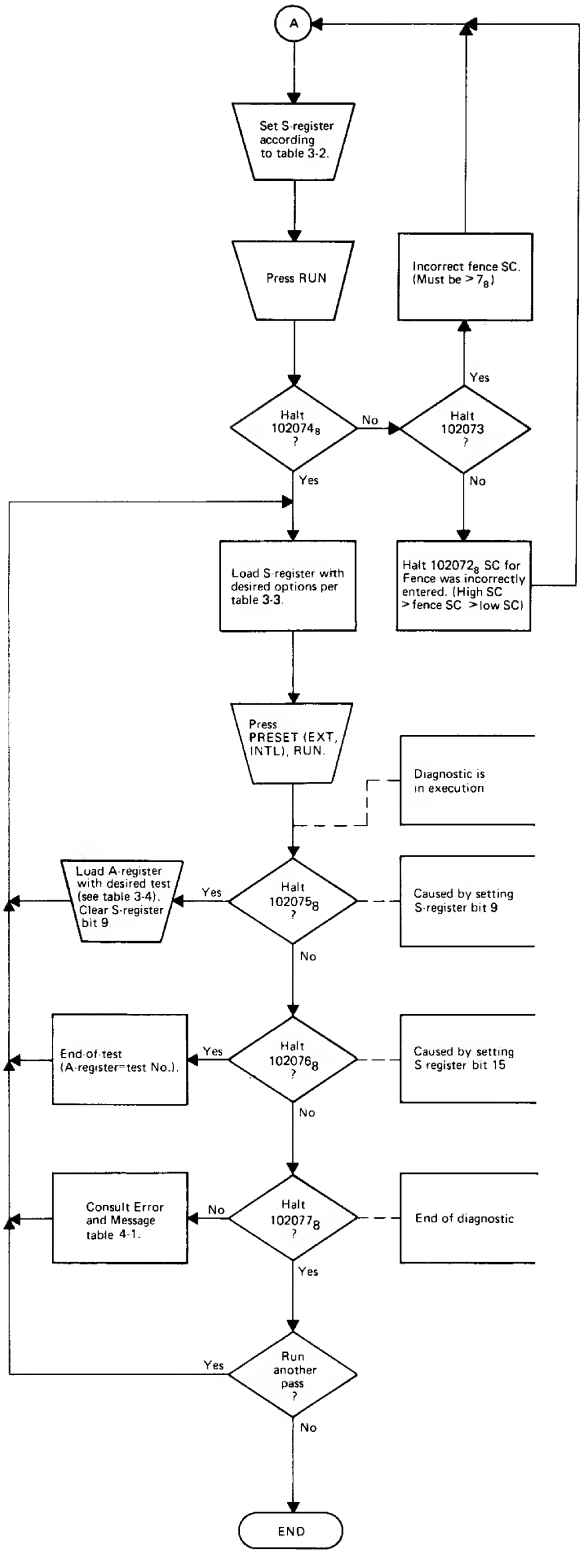


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Figure 3-1. Operating Procedure Flowchart (Sheet 2 of 2)

Table 3-2. Entry of Privileged Interrupt Fence SC via Switch Register

S-REG BIT	FUNCTION
15-6	Reserved.
5-0	SC of privileged interrupt fence. (The following condition must be met: high SC > fence > low SC.)

Table 3-3. Desired Test Options via Switch Register

S-REG BIT	MEANING IF SET
15	Halt 102076 (octal) at the end of each test. The A-Register contains the test number in octal.
14	Suppress error halts.
13	Loop on last test section being executed.
12	Loop on diagnostic.
11	Suppress error messages.
10	Suppress information messages.
9	Abort diagnostic execution after the current test section and halt (102075). Operator can specify a new group of test(s) in the A-Register. Then clear Switch Register bit 9 and press RUN.
8	Suppress operator intervention tests.
7-0	Reserved.

Table 3-4. Test Selection Summary via A-Register

A-REG BIT	IF SET WILL EXECUTE*	TEST
0	High SC Interrupt Test	00
1	Low SC Interrupt Test	01
2	Set Control/Clear Control Fence Channel Test	02
3	Clear Control and Flag With Preset Test	03
4	No Action: Flag and Control Cleared Test	04
5	High SC: Flag Cleared and Control Set Test	05
6	High SC: Flag and Control Set Test	06
7	High SC and Interrupt: Flag Set and Control Cleared Test	07
8	Low SC/Fence Priority Test	08
9	Scope Loop Test (Not part of standard tests.)	09

*If all A-register bits are cleared, Tests 00-08 will be executed.

Table 3-2. Entry of Privileged Interrupt Fence SC via Switch Register

S-REG BIT	FUNCTION
15-6	Reserved.
5-0	SC of privileged interrupt fence. (The following condition must be met: high SC > fence > low SC.)

Table 3-3. Desired Test Options via Switch Register

S-REG BIT	MEANING IF SET
15	Halt 102076 (octal) at the end of each test. The A-Register contains the test number in octal.
14	Suppress error halts.
13	Loop on last test section being executed.
12	Loop on diagnostic.
11	Suppress error messages.
10	Suppress information messages.
9	Abort diagnostic execution after the current test section and halt (102075). Operator can specify a new group of test(s) in the A-Register. Then clear Switch Register bit 9 and press RUN.
8	Suppress operator intervention tests.
7-0	Reserved.

Table 3-4. Test Selection Summary via A-Register

A-REG BIT	IF SET WILL EXECUTE*	TEST
0	High SC Interrupt Test	00
1	Low SC Interrupt Test	01
2	Set Control/Clear Control Fence Channel Test	02
3	Clear Control and Flag With Preset Test	03
4	No Action: Flag and Control Cleared Test	04
5	High SC: Flag Cleared and Control Set Test	05
6	High SC: Flag and Control Set Test	06
7	High SC and Interrupt: Flag Set and Control Cleared Test	07
8	Low SC/Fence Priority Test	08
9	Scope Loop Test (Not part of standard tests.)	09

*If all A-register bits are cleared, Tests 00-08 will be executed.

DIAGNOSTIC PERFORMANCE

SECTION IV

4-1. TEST DESCRIPTION

The HP 12936 Privileged Interrupt Fence Diagnostic consists of nine tests and a trouble-shooting loop test. The nine tests perform a go/no-go test of the fence. When an error is detected, Test 09 of the diagnostic, the scope loop test, may be executed to observe FLAG, CONTROL, and IRQ states.

Testing of the fence is based on the four operating states of the fence.

The tests provided by this diagnostic are:

Test	Function Tested
00	High SC Interrupt Test
01	Low SC Interrupt Test
02	Set CONTROL/Clear CONTROL Fence Channel Test
03	Clear CONTROL and FLAG With Preset Test
04	No Action: FLAG and CONTROL Cleared Test
05	High SC: FLAG Cleared and CONTROL Set Test
06	High SC: FLAG and CONTROL Set Test
07	High SC and Interrupt: FLAG Set and CONTROL Cleared Test
08	Low SC/Fence Priority Test
09	Scope Loop Test

4-2. TEST 00 — HIGH SELECT CODE INTERRUPT

The ability of the high SC (low priority channel) to interrupt is tested. The FLAG and CONTROL of the channel is set and the interrupt system turned on. The channel should interrupt but if it does not, error message E035 will occur.

4-3. TEST 01 — LOW SELECT CODE INTERRUPT

The ability of the low SC (high priority channel) to interrupt is tested. The FLAG and CONTROL of the channel is set and the interrupt system turned on. The channel should interrupt but if it does not, error message E036 will occur.

4-4. TEST 02 — SET CONTROL/CLEAR CONTROL FENCE CHANNEL TEST

The ability of the I/O instruction CLC FCH (FCH = fence SC) to clear fence CONTROL is tested. This is done by setting the high SC (low priority channel) to interrupt and by setting the fence CONTROL and clearing the fence FLAG followed by turning on the interrupt system. With the fence CONTROL set and FLAG cleared, priority to the high SC should be denied. When the CLC FCH instruction is executed, the fence CONTROL should clear, resulting in the high SC interrupt.

If the high SC does not interrupt, error message E030 will occur.

If the fence channel interrupts (fence FLAG and CONTROL set), error message E031 will occur.

4-5. TEST 03 — CLEAR CONTROL AND FLAG WITH PRESET

The ability of EXTERNAL PRESET to clear the fence CONTROL and FLAG is tested. This is done by setting fence FLAG and CONTROL which lowers the priority, followed by message H032.

When RUN is pressed, the program sets the high SC (low priority channel) to interrupt and turns on the interrupt system. Since EXTERNAL PRESET clears fence FLAG and CONTROL, the high SC should interrupt.

If the high SC does not interrupt, error message E033 results.

If the fence CONTROL is cleared, but FLAG does not clear, then the fence will interrupt resulting in error message E034.

4-6. TEST 04 — NO ACTION: FLAG AND CONTROL CLEARED

This test checks that with the fence FLAG and CONTROL cleared, the high SC (low priority channel) is not denied priority and that the fence does not interrupt. This is done by setting the low and high SC's to interrupt. If the PCA is functioning properly, the low SC should interrupt, followed by the high SC.

If the low and high SC's fail to interrupt, error message E040 results.

If the high SC fails to interrupt after the low SC, error message E043 results.

Finally, if the high SC interrupts before the low SC, error message E044 results.

4-7. TEST 05 — HIGH SELECT CODE: FLAG CLEARED AND CONTROL SET

This test checks that with the fence FLAG cleared and CONTROL set, the high SC (low priority device) may be denied priority while the low SC (high priority channel) may still

interrupt. This is done by setting the low and high SC's to interrupt. If the PCA is functioning properly, only the low SC should interrupt.

If the low SC does not interrupt, error message E050 results.

If the fence interrupts before the low SC, error message E051 results.

If the fence interrupts after the low SC, error message E052 results.

If the high SC interrupts before the low SC, error message E053 results.

If the high SC interrupts after the low SC, error message E054 results.

4-8. TEST 06 — HIGH SELECT CODE: FLAG AND CONTROL SET

This test is basically the same as test 5 with the only difference being the fence FLAG is set as well as the CONTROL.

If the low SC does not interrupt, error message E060 results.

If the fence interrupts before the low SC, error message E061 results.

If the fence interrupts after the low SC, error message E062 results.

If the high SC interrupts before the low SC, error message E063 results.

If the high SC interrupts after the low SC, error messasge E064 results.

4-9. TEST 07 — HIGH SELECT CODE AND INTERRUPT: FLAG SET AND CONTROL CLEARED

This test checks that with the fence FLAG set and CONTROL cleared, that the fence denies priority to the high SC (low priority channel) and that it will interrupt. This is done by initially setting the high SC and fence to interrupt. If the PCA is functioning properly, the fence will interrupt. If the fence interrupts properly, the low SC (high priority channel) is set to interrupt and the fence lowered. The low SC followed by the high SC should now interrupt.

If the fence or high SC fail to interrupt, error message E100 results.

If the low SC fails to interrupt after fence, error message E103 results.

If the high SC fails to interrupt after the low SC, error message E101 results.

If the low SC interrupts before the fence, error message E102 results.

If the high SC interrupts before either the fence or low SC interrupts, error message E104 results.

If the high SC interrupts after the fence interrupts, but before the low SC interrupts, error message E105 results.

4-10. TEST 08 — LOW SELECT CODE/FENCE PRIORITY

This test checks that with the fence FLAG and CONTROL set that the low SC (high priority channel) can deny priority to the fence. If the PCA is functioning properly, the low SC should interrupt followed by the fence.

If the fence or high SC fail to interrupt, error message E200 results.

If the fence fails to interrupt after the low SC, error message E201 results.

If the fence interrupts before the low SC, error message E202 results.

4-11. TEST 09 — SCOPE LOOP

This section provides a scope loop on the fence PCA. The loop consists of the following sequence of I/O instructions.

```
STC   FCH      set control
OTA   FCH      set flag
CLC   FCH      clear control
CLF   FCH      clear flag
STF   0        turn on int system
STC   FCH      set control
OTA   FCH      set flag
CLC   FCH      clear control
CLF   FCH      clear flag
CLF   0        turn off int system

(loop to first instruction)
```

A small time delay precedes each I/O instruction. To exit this loop, bit 9 of the S-register is set followed by clearing bit 9 of the A-register.

4-12. DIAGNOSTIC MESSAGES AND HALTS

The diagnostic communicates to the operator through the console, halts, or both, based on configuration and switch register settings. Thus, messages consist of halt codes (T- and A-register values) and/or text on the console.

There are two general categories of messages output to the operator: program/operator communication messages and test failure (error) messages. Table 4-1 lists messages and halt

codes. Messages coded with the leter "H" identify them as communication messages. All error messages are coded with the letter "E".

The test that outputs each message is indicated in the table. The tests are described in this manual under the heading "Test Descriptions".

"TC" refers to the Test Control routine.

"CF" refers to the select code configuration routine contained in this diagnostic.

Table 4-1. Error Information Messages and Halt Codes

HALT CODE	TEST SECTION	MESSAGE	COMMENTS
102070	CF	None	Select codes entered for high and low channel are valid; enter privileged interrupt fence select code into Switch Register bits 0 to 5; press RUN.
102071	CF	None	Select codes entered for high or low SC interface PCA's were invalid; reenter high and low select codes (SC>7) into Switch Register; bits 11-6 and 5-0 (high SC must be ≥ low SC + 2); press RUN.
102072	CF	None	Select code entered for fence is invalid; reenter select code into Switch Register bit 5-0 (high SC > fence SC > low SC); press RUN.
102073	CF	None	Select code of privileged interrupt fence, high, or low SC interface PCA was invalid; reenter valid select code (SC>7); press RUN.
102074	CF	None	Select code of privileged interrupt fence was valid; enter program options into Switch Register (table 3-3); press RUN.
102075	TC	None	Test select halt which resulted from switch 9 being set; enter selection of tests to be executed into A-register; set bit *i* to select test *i*; A-register = 0 selects *all* tests to be executed except Test 09.
102076	TC	None	End of test section halt resulting from switch 15 being set; A-register holds test section number just completed; press RUN to begin next test section.
None	TC	12936 PRIVILEGED INTERRUPT CARD DIAGNOSTIC	Introductory message.

Table 4-1. Error Information Messages and Halt Codes (Continued)

HALT CODE	TEST SECTION	MESSAGE	COMMENTS
None	TC	TEST *nn*	Indicates to which test a list of error messages, which follow, belongs; *nn* = test number.
102077	TC	PASS *nnnnnn*	All selected test sections of the diagnostic have completed; *nnnnnn* is the octal number of passes completed and is contained in the A-register, if the halt is invoked (switch 12 clear).
106077	TC	None	Halt stored in CPU memory locations 2_8 to 77_8 to trap interrupts which occur unexpectedly because of hardware malfunctions; M-register contains the I/O slot which interrupted; correct problem and reload diagnostic before continuing with diagnostic.
102030	02	E030 CLC SC FAILED TO CLEAR CONTROL OR PRIORITY CHAIN BROKEN	The Clear Control I/O instruction failed to clear the fence CONTROL; the fence was set to deny priority to the high SC; the CLC instruction execution should have allowed the high SC to interrupt.
102031	02	E031 CLC SC CAUSED FLAG TO SET	The CLC instruction resulted in setting the fence FLAG as well as clearing fence CONTROL; this caused the fence to interrupt erroneously.
102032	03	H032 PRESS PRESET (EXT), RUN	Press PRESET (EXTERNAL PRESET); press RUN.
102033	03	E033 PRESET (EXT) FAILED TO CLEAR CONTROL AND-OR FLAG OR PRIORITY CHAIN BROKEN	The PRESET (EXTERNAL PRESET) failed to clear fence CONTROL and/or its FLAG; the high SC is set to interrupt but is also denied priority while the fence CONTROL and FLAG are set; if PRESET clears the FLAG and CONTROL, the high SC should interrupt unless the priority chain is broken.
102034	03	E034 FENCE INT'D AFTER PRESET (EXT)	PRESET cleared CONTROL but not the fence FLAG; an erroneous interrupt resulted.
102035	00	E035 HI SC SET TO INT BUT DID NOT INT	High SC was set to interrupt but did not. Check the priority chain and the high SC PCA.
102036	01	E036 LO SC SET TO INT BUT DID NOT INT	Low SC was set to interrupt but did not. Check the priority chain and the low SC PCA.
102040	04	E040 NO INT RECEIVED FROM LO OR HI SC	The high and low SC's did not interrupt.

Table 4-1. Error Information Messages and Halt Codes (Continued)

HALT CODE	TEST SECTION	MESSAGE	COMMENTS
102041	04	E041 HI SC DID NOT INT AFTER LO SC	High SC failed to interrupt after the low SC interrupted.
102042	04	E042 FENCE INT'D BEFORE LO SC INT'D BUT FENCE FLAG NOT SET	Fence should not interrupt but did interrupt before the low SC.
102043	04	E043 FENCE INT'D AFTER LO SC INT'D BUT FENCE FLAG NOT SET	Fence should not interrupt but did after low SC.
102044	04	E044 HI SC INT'D BEFORE LO SC	The high SC channel interrupted before the low SC.
102050	05	E050 NO INT RECEIVED FROM LO SC	The high and low SC's are set to interrupt, but only the low SC should interrupt because the fence is up; no interrupt was received from low SC.
102051	05	E051 FENCE INT'D BEFORE LO SC WITH FENCE CONTROL SET	Fence should not interrupt but did interrupt before low SC.
102052	05	E052 FENCE INT'D AFTER LO SC INT'D WITH FENCE CONTROL SET	Fence should not interrupt but did interrupt after the low SC.
102053	05	E053 LO SC DID NOT INT BUT HI SC INT'D WITH FENCE UP	High SC should not interrupt but did interrupt before low SC.
102054	05	E054 HI SC INT'D AFTER LO SC INT'D BUT FENSE WAS UP	High Sc should not interrupt but did interrupt after low SC.
102060	06	E060 NO INT RECEIVED FROM LO SC	The high and low SC's are set to interrupt while the fence FLAG and fence CONTROL are set; only the low SC should interrupt since the fence is up; but the low SC did not interrupt.
102061	06	E061 FENCE INT'D BEFORE LO SC BUT FENCE FLAG AND CONTROL SET	Fence should not interrupt but did interrupt before the low SC.
102062	06	E062 FENCE INT'D AFTER LO SC INT'D BUT FLAG AND CONTROL SET	Fence should not interrupt but did after the low SC.
102063	06	LO SC DID NOT INT BUT HI SC INT'D WITH FENCE UP	High SC should not interrupt but did interrupt before the low SC.
102064	06	E064 HI SC INT'D AFTER LO SC INT'D BUT FENCE UP	High SC should not interrupt but did interrupt after the low SC.

Table 4-1. Error Information Messages and Halt Codes (Continued)

HALT CODE	TEST SECTION	MESSAGE	COMMENTS
106000	07	E100 NO INT RECEIVED FROM FENCE OR HI SC	The high SC and fence are initially set to interrupt with the fence FLAG set and fence CONTROL clear; the fence should interrupt with high SC denied priority; if so, the low SC is set to interrupt and the fence FLAG cleared; the fence and high SC did not interrupt initially.
106001	07	E101 HI SC DID NOT INT AFTER LO SC	The high SC failed to interrupt after the low SC.
106002	07	E102 LO SC INT'D BEFORE FENCE	The low SC was not set to interrupt but did interrupt before the fence.
106003	07	E103 LO SC DID NOT INT AFTER FENCE	The low SC was set to interrupt after the fence but did not interrupt.
106004	07	E104 HI SC INT'D BUT FENCE AND LO SC DID NOT INT	Fence and low SC failed to interrupt, but high SC did interrupt; fence failed to deny priority to high SC.
106005	07	E105 HI SC INT'D AFTER FENCE INT'D BUT BEFORE LO SC INT'D	High SC interrupted after the fence, but the low SC should have interrupted.
106010	08	E200 NO INT RECEIVED FROM FENCE OR LO SC	No interrupt was received when an interrupt was expected, first from the low SC, then from the fence.
106011	08	E201 FENCE DID NOT INT AFTER LO SC	The fence did not interrupt after the low SC interrupted.
106012	08	E202 FENCE INT'D BEFORE LO SC	The low SC should interrupt before the fence but the fence interrupted first.
106070 thru 106076			Configurator halts. Refer to Diagnostic Configurator Manual.

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